AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

Claim 1. (currently amended) A diagnostic compiler for use with a pipeline analog-to-digital converter (ADC) having code sequences corresponding to stages thereof, comprising:

a transition locator configured to apply a mathematical function to determine transition locations for said code sequences based on said stages and the number of bits in respective ones of said stages ~~a design~~ of said pipeline ADC; and

a characteristics indicator coupled to said transition locator and configured to provide at least one characteristic of said pipeline ADC based on said transition locations.

Claim 2. (currently amended) The diagnostic compiler as recited in Claim 1 wherein the mathematical function said transition locator ~~determination of transition locations~~ is configured to apply to determine said transition locations is ~~employ~~ a Bohan function ~~mathematical function based on said stages~~.

Claim 3. (currently amended) The diagnostic compiler as recited in Claim 2 wherein said Bohan ~~mathematical~~ function is ~~configured to employ an attribute selected from the group consisting of~~:

$$LST_m \quad \frac{N}{2} \quad \frac{N}{2^{m\ 2}} \quad j \quad \frac{N}{2^{m\ 1}} \ ,$$

where LST_m is the location of stage transitions, m is the stage, N denotes 2^n for an n-bit converter and j is defined by $0 \leq j \leq 2^m-2$

~~orthogonality, and~~

~~bi-state functionality~~.

Claim 4. (original) The diagnostic compiler as recited in Claim 1 wherein said at least one characteristic is configured to represent a stage mismatch error of said ADC.

Claim 5. (original) The diagnostic compiler as recited in Claim 4 wherein said stage mismatch error is configured to contain an attribute selected from the group consisting of:

capacitive mismatch,

resistive mismatch, and

comparative mismatch.

Claim 6. (original) The diagnostic compiler as recited in Claim 1 wherein said at least one characteristic is configured to represent an offset error of said ADC.

Claim 7. (original) The diagnostic compiler as recited in Claim 1 wherein said at least one characteristic is configured to represent a superposition error of said ADC.

Claim 8. (currently amended) A method of compiling for use with a pipeline analog-to-digital converter (ADC) having code sequences corresponding to stages thereof, comprising:

Applying a mathematical function to determine ~~determining~~ transition locations for said code sequences based on said stages and the number of bits in respective ones of said stages ~~a design~~ of said pipeline ADC; and

providing at least one characteristic of said pipeline ADC based on said transition locations.

Claim 9. (currently amended) The method as recited in Claim 8 wherein said step of determining transition locations is performed by applying a Bohan function based on said stages and the number of bits in respective ones of said stages ~~employs a mathematical function based on said stages~~.

Claim 10. (currently amended) The method as recited in Claim 9 wherein said Bohan function is ~~mathematical function employs an attribute selected from the group consisting of~~:

$$LST_m \quad \frac{N}{2} \quad \frac{N}{2^{m\ 2}} \quad j \quad \frac{N}{2^{m\ 1}} \ ,$$

where LST_m is the location of stage transitions, m is the stage, N denotes 2^n for an n-bit converter and j is defined by $0 \leq j \leq 2^m - 2$

~~orthogonality, and~~

~~bi-state functionality~~.

Claim 11. (original) The method as recited in Claim 8 wherein said providing at least one characteristic represents a stage mismatch error of said ADC.

Claim 12. (original) The method as recited in Claim 11 wherein said stage mismatch error contains an attribute selected from the group consisting of:

capacitive mismatch,

resistive mismatch, and

comparative mismatch.

Claim 13. (original) The method as recited in Claim 8 wherein said providing at least one characteristic represents an offset error of said ADC.

Claim 14. (original) The method as recited in Claim 8 wherein said providing at least one characteristic represents a superposition error of said ADC.

Claim 15. (currently amended) A test system, comprising:

a data processing unit that has a device testing interface;

a pipeline analog-to-digital converter (ADC) that is coupled to said device testing interface and has code sequences corresponding to stages thereof; and

a diagnostic compiler that is coupled to said pipeline ADC, including:

a transition locator that determines transition locations for said code sequences by applying a mathematical function based on said stages and the number of bits in respective ones of said stages ~~a design~~ of said pipeline ADC; and

a characteristics indicator, coupled to said transition locator, that provides at least one characteristic of said pipeline ADC based on said transition locations.

Claim 16. (currently amended) The system as recited in Claim 15 wherein the mathematical function said transition locator ~~determination of transition locations~~ employs is a Bohan function ~~a mathematical function based on said stages~~.

Claim 17. (currently amended) The system as recited in Claim 16 wherein said Bohan ~~mathematical~~ function is ~~employs an attribute selected from the group consisting of~~:

$$LST_m \quad \frac{N}{2} \quad \frac{N}{2^{m\ 2}} \quad j \quad \frac{N}{2^{m\ 1}} \ ,$$

where LST_m is the location of stage transitions, m is the stage, N denotes 2^n for an n-bit converter and j is defined by $0 \leq j \leq 2^m-2$

~~orthogonality, and~~

~~bi-state functionality~~.

Claim 18. (original) The system as recited in Claim 15 wherein said at least one characteristic represents a stage mismatch error of said ADC.

Claim 19. (original) The system as recited in Claim 18 wherein said stage mismatch error contains an attribute selected from the group consisting of:

capacitive mismatch,

resistive mismatch, and

comparative mismatch.

Claim 20. (original) The system as recited in Claim 15 wherein said at least one characteristic represents an offset error of said ADC.

Claim 21. (original) The system as recited in Claim 15 wherein said at least one characteristic represents a superposition error of said ADC.